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TapClock

Tempo/Beat Generator

New firmware

This document describes the specifications and operation of a new firmware for the Plan B Tap Clock. This new firmware provides enhanced synchronization with externally applied clock signals.

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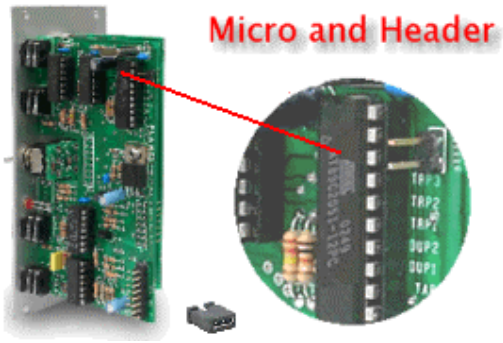
Section One – Installing the New Firmware

Retrofit Overview

This new firmware is programmed into the microcontroller that is the heart of the Tap Clock module. As such, the original processor needs to be exchanged with one that has been programmed to this new firmware level.

Note:
Those unfamiliar with the task should seek out an experienced individual to perform the upgrade.



This new firmware takes advantage of a 2-pin header on the PCB to encode whether the module is in Standard or Sync Mode. If this header is "strapped" (by placing a "shunt" or shorting plug onto the pins), the module immediately enforces the Sync Mode. When removed, the module immediately returns to Standard Mode.

This header is behind the panel and not readily accessible. The figure left indicates the location for both the microcontroller, which needs to be changed, and the 2-pin header.

First Steps:

Naturally, the replacement of the microcontroller cannot occur under power.

The removal of the original microcontroller and the insertion of a newly programmed one, invokes the need to avoid bending or misaligning microcontroller pins. This operation is not likely done with unaided hands and requires a tool.

Commonly available tools, for the removal and insertion of integrated circuits, depict left (Radio Shack Model: 276-1581 Catalog #: 276-1581). Perhaps not unsurprising is the most common tool for the careful removal of a DIP integrated circuit, the Excelite “green”.


Probably the most common DIP integrated circuit removal tool.

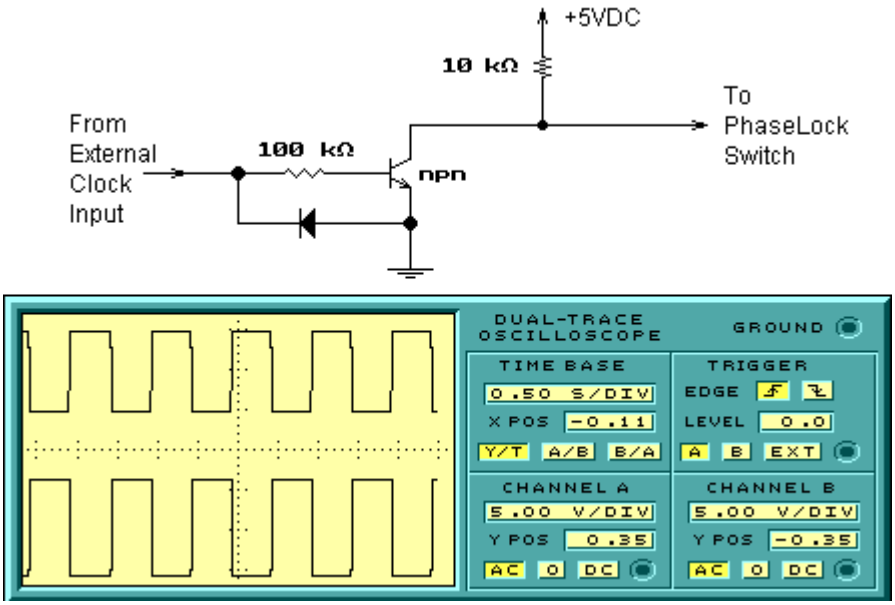
If using a thin flat screwdriver, the integrated circuit is pried out of its socket with gentle insertions between the integrated circuit and its socket. These insertions occur at one end and then the other in an alternating fashion. This is, in essence, a slow, gentle rocking which causes the integrated circuit to retreat from the socket.

The prying action is a slow, careful and gentle operation not requiring much pin movement for each alternating action.

Section Two – Applying an External Clock

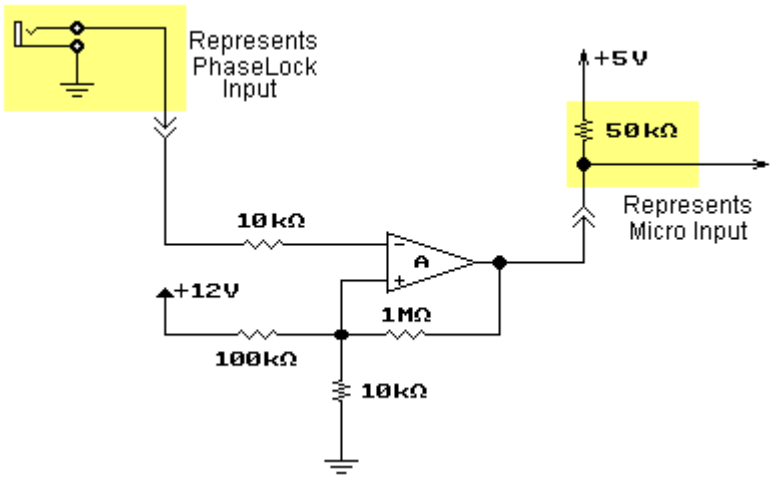
Adding a Simple Inverter

A single transistor can accomplish the signal inversion required for this firmware revision. This isn't an all purpose circuit, but is fairly general in that signals ranging from as little as 0 to 3V will invert.



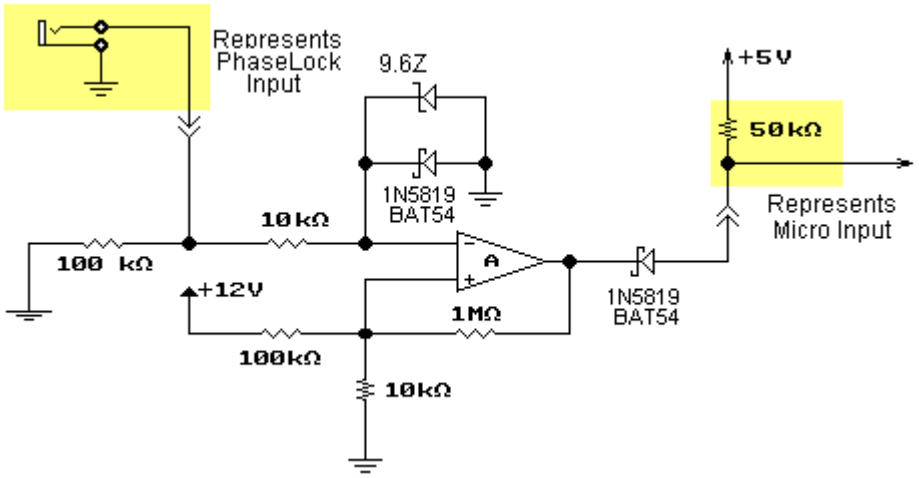
Fashioning an "On-Board" Comparator

A simple circuit for conditioning an external clock, for use with the new firmware upgrade, depicts below. This circuit is a simple comparator that switches low when the input clock exceeds approximately +1 volt. The central switching point is approximately +1 VDC and there is a window of approximately a .1 volt for hysteresis to ensure smooth transitioning when a slower sloped clock input is applied to the module.



Similar to how the circuit above tolerates a variety of

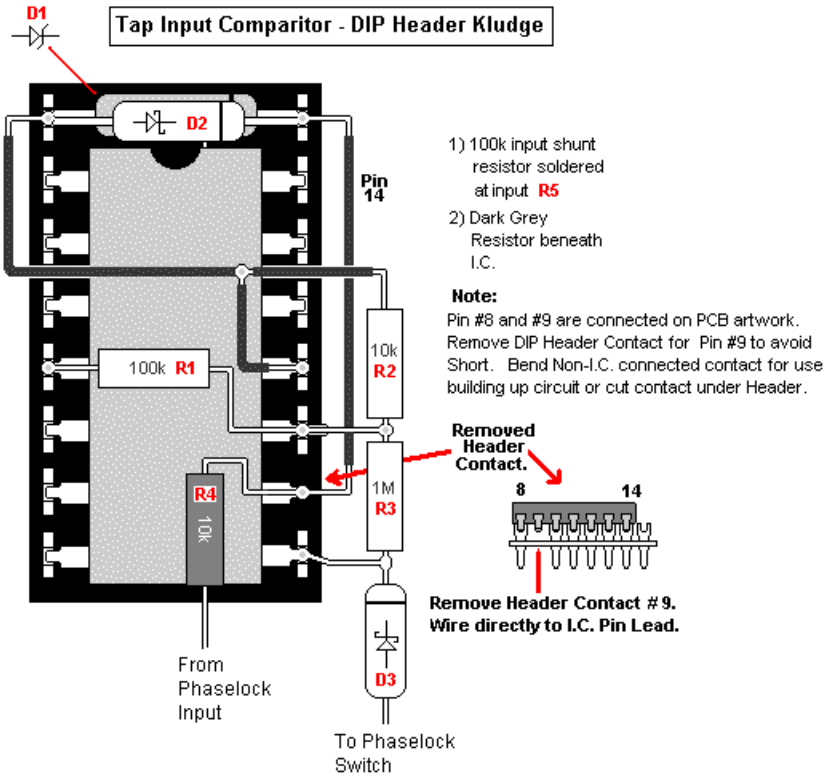
external clock waveforms, protection must be provided to ensure signals outside of the range of tolerance for the Tap Clocks LM324 integrated circuit. The more developed circuit below ensures signals that swing below -.3 volts or above +10 volts do not cause the LM324 op-amp or the connected microcontroller, to mis-operate.



Zener and schottky diodes ensure the voltage of the external clock signal never exceeds either +10 or -.3 volts in amplitude at the negative input of the comparator circuit. The connected microcontroller is isolated by a schottky diode which is reversed biased when the comparator presents +12 volts at output. When the comparator presents a low output (~0 volts), the forward biased schottky diode pulls the microcontroller input low (+.3 volts) to activate timing recognition. Finally, the circuit presents a traditional 100k input impedance expected for a modular synthesizer input.

Hardware Realization

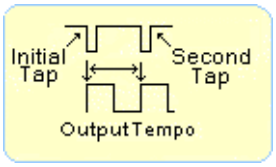
The graphic below depicts an idealized method for implementing the comparator circuit in a stock Tap Clock.



The comparator is mostly built upon a 16 contact D.I.P. header that plugs into a socket on the Model 28 Jack Board. This area of the board is very tight and great care is needed to both remove the existing LM324 and replace it with the constructed D.I.P. header.

Section Three: Modes of Operation

Entering Standard Mode Operation



Whenever, there is no jumper installed the Tap Clock performs with the Standard Mode, just as the original firmware for the Tap Clock.

In this mode the Tap Clock attempt to mimic the duration between two Tap-Tap activations by outputting pulse at the discriminated rate.

The figure right attempts to depict the relation between two sequential panel switch activations and the echo of its duration as emulated on output.

as the period between sequential "low going" input signals (a natural result of panel switch electronics). The Tap Clock emits pulses with a tempo correlating to the period between these two manual switch activations

is an idealized representation of the Tap switch and how it looks to the design electronics. When no button is pressed a "high" value is presented. Once pressed, the switch presents a "low" value.

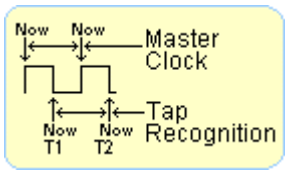
Synchronous Mode

When the Tap Clock input panel switch is set to Phase lock, externally applied clock pulses replace manual Tap-Tap panel operations.

Entering Sync Mode

The Tap Clock circuit recognizes external pulses when they go from positive to negative. Sync Mode measures the time between two of these sequential low going edges.

For phase coherent synchronization, an External Input should invert prior to connection to the Tap Clock.



The graphic right depicts idealized Master Clock input (if not inverted) and its relation to Tap Cycle recognition. This second image indicates how the module as 50% duty-cycle frequency rate adopts the time between first “falling edge” and the second “falling edge”. The first low going edge starts timing that continues until the detected falling edge. The period of time between these edges is used to set the timing from which the *times* 1, *times* 2, and *times* 3, output frequencies are generated.

the

next

base

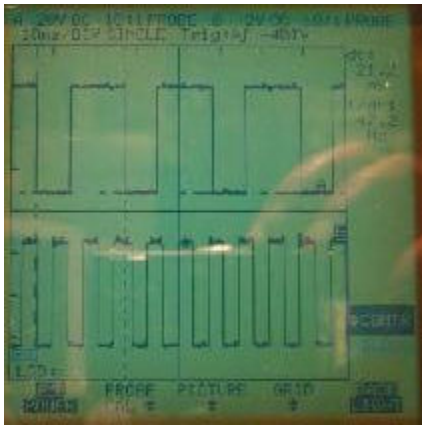
Using Sync Mode

Inverting an External Input corrects for low going edge recognition and, when accompanied by activation of the sync mode, enables the most accurate phase agreement the module can provide.

Section Four – Specifications

Images

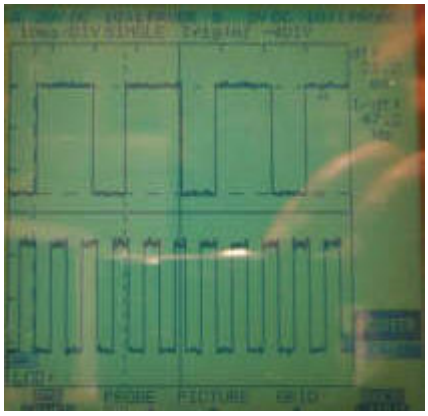
To best indicate the operability of the new alpha code revision, a series of oscilloscope pictures were taken and are reproduced with a description for what they depict.



The amateur photo left, depicts the Tap Clock external input (47Hz) (in the top of the frame), and the Tap Clocks Triple output (lower portion of the frame). The input is the output of a simple NE555 timer and the typical lack of 50/50 duty cycle is evident. This frequency is shown as it exceeds the published specification for the module and demonstrates a worst case.

Recalling that the falling edge of external input causes timing, it is the second set of triple outputs which are the result of the incoming pulse. The degree of general conformance (although delayed) as well as the lack of synchronization is clearly evident. The 'dotted' vertical lines are the cursor that generates the frequency depicted on the right of the waveform display.

The second photo left depicts the approximately the same input frequency but this time the Tap Clock is instructed to 'Synchronize' with the incoming external pulse.



Since the Tap Clock detects timing on the 'falling edge' of incoming pulse widths, a 'correction can be seen where the width of one the triplet pulses is shortened to achieve synchronization with the incoming signal. To indicate to the Tap Clock that synchronization is required Pin #3 (designated as P3.2) is held to a logic low level. The effect of being in or out of synchronization is clearly audible. Although widths can be shortened in 'Synch Mode' the number of clock pulses per period is correct and thus correct timing will occur.

A short movie file has been made which allows the incoming and outgoing waveforms to be acoustically heard while the waveforms display at differing frequencies and across the two modes, depict. Poorly, recorded some noise modulation depicts on the scope. Ignoring this, it might be interesting to the listener to notice how changes in the incoming frequency provoke the module to 'catch up'. Unlike a Phase Lock Loop the module does not 'overshoot' instead it migrates to the new value and stops.

Section Five – User Modifications

Signal Inversion

For the intrepid, there are two alternative hardware modifications that would integrate the clock signal inversion required to best exploit the new firmware revision.

The second modification replaces the existing single pole Tap/Phase Lock switch with a dual pole switch. The additional pole replaces the manual shunt causing Sync Mode to occur when ever in PhaseLock mode. When switched to Tap the Standard Mode occurs (restoring original Tap Mode functionality). Further revisions of this page will publish the 'steps to complete' for these modifications.