GREAT DIVIDE & 8-BIT CIPHER Build Manual (02/12/11)

nonlinearcircuits

MODULE DESCRIPTION:

The Great Divide simply takes an input signal and divides it by 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192 and 16384. There is a reset input as well. The clock and rest inputs can be supplied with any signal that crosses approx. 1.1V. It is not a particularly elaborate circuit but quite useful and VERY useful to use as a data source for the 8-bit Cipher. There are LEDs for the final 8 stages, but outputs for every stage.

The 8-bit Cipher is a somewhat dumbed-down version of the Buchla SOU with gate outputs for each of the 8 stages. The CV outputs are all interconnected giving 4 different but related patterns.

The Cipher has a clock input and two data inputs; again these can be fed anything crossing 1.1V. To get it to work it must have a signal on the data input to feed the shift registers and it must have a clock signal to shift the data thru the stages. To put it simply, just feed it two LFO signals and see what happens.

You cannot feed the gate outputs directly into the data inputs, well you can but it will eventually end up with all stages 'on' and stay like that. Feed the gate outputs into some logic gates or the Great Divide and then put those outputs into the data input.

BUILDING IT:

The set of three PCBs are designed to connect together using two sets of 40 pin connectors

At Futurlec these are

FHEADD40 40 Pin .100 Straight Female Double Headers

and

HEADRAD40 40 Pin .100 Right Angle Double Headers

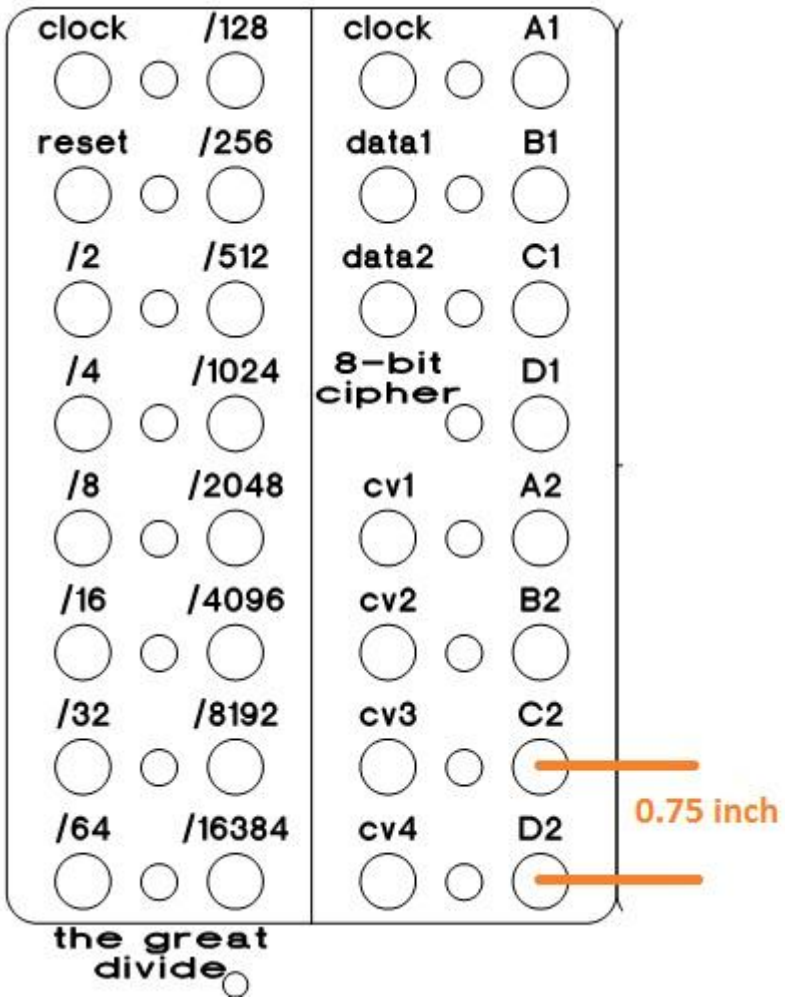
I will get some photos of a finished build on http://www.sdiy.org/pinky/data/data.html soon or check out the video in the original thread on these circuits at Muffs.

LEDs are mounted directly on the breakout boards and inserted into LED holders on the panel. Jacks are connected to the breakout boards using wire clippings. There is a single hole on the main PCB to hold it in place with a stand-off to the panel. The combination of 16 LEDs mounted on the panel, 31 jacks connected by clippings, two 40 pin connectors and a standoff; results in a stable and strong mount for the PCB…..providing you don't sit on it.

The panel design is below, it is not to scale. If you want the FrontPanelExpress file, pm/email me.

Basically there are 8 jacks per column spaced 0.75 inch apart. The jack columns are spaced 1 inch apart. The two LED columns are 0.5 inch from each jack column (ie. in the middle)

The third column has just 7 jacks (where "8-bit cipher" is written)



REFER TO THE SILKSCREEN IMAGE BELOW FOR THESE COMMENTS

There are 4 regular diodes marked below in red, 1N4148 are fine. It is a bit hard to see on the PCB but there is an arrow indicating direction

Anode ➡ Cathode

Here is the main info

All resistors marked with a "+" are 1k

All unmarked resistors are 100k

All unmarked capacitors are for decoupling; 100nF would suitable

Except for the two 10uF electros, there are two 'marked' capacitors, on the right side above the 40 pin connector, is a 10nF. Next to the 4015 is a 1nF cap.

The decoupling caps have a tight spacing of 2.5mm, I use these ones from Futurlec:

C100UC 0.1uF 50V Ceramic Capacitors

All transistors are NPN, the pinouts suit BC547. Any general purpose transistor will work.

A few transistors have “ebc” to indicate the pinout.

There are two 1N4004 diodes near the power connector. These are to protect against the power being connected wrongly, leave them off if you like. They do nothing in normal operations.

I circled two 10k resistors in green as the “10k” labels are a little too close to nearby unmarked 100k resistors so that it may be unclear. So the two in the circle are 10k, the two resistors, above and to the right of the green circle, are 100k.

Very rough, incomplete BOM

chips:

4015

4024 x 2

TL072 x 2

TL074 x 2

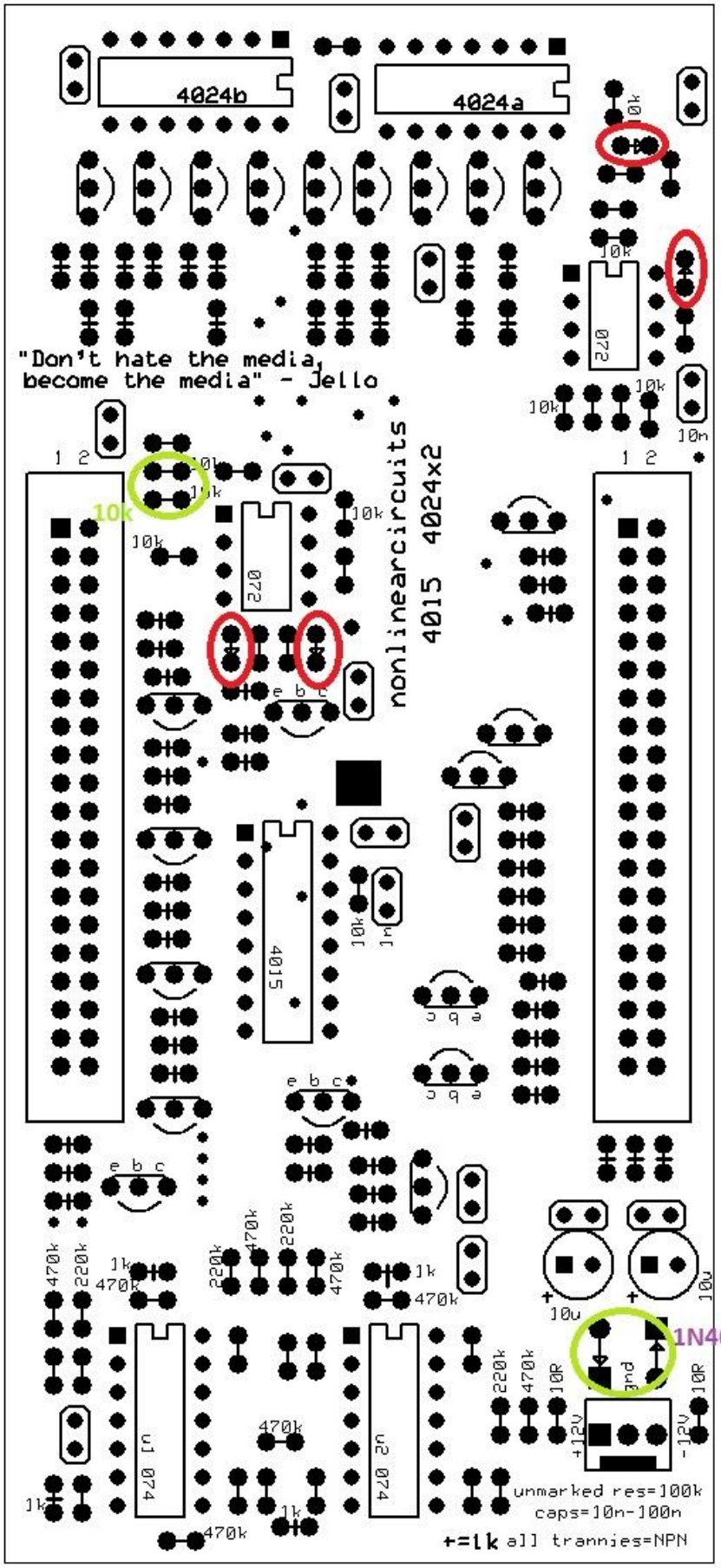
other bits:

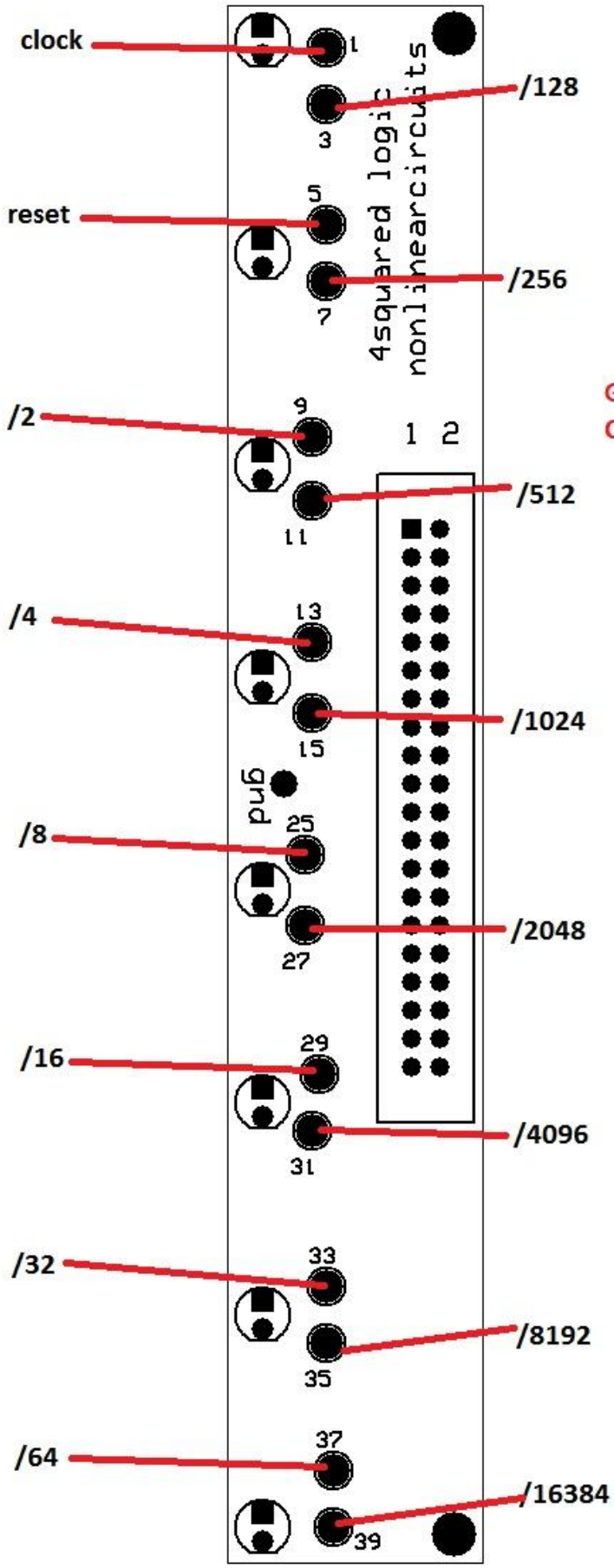
About 22 transistors

something like 70 1k resistors

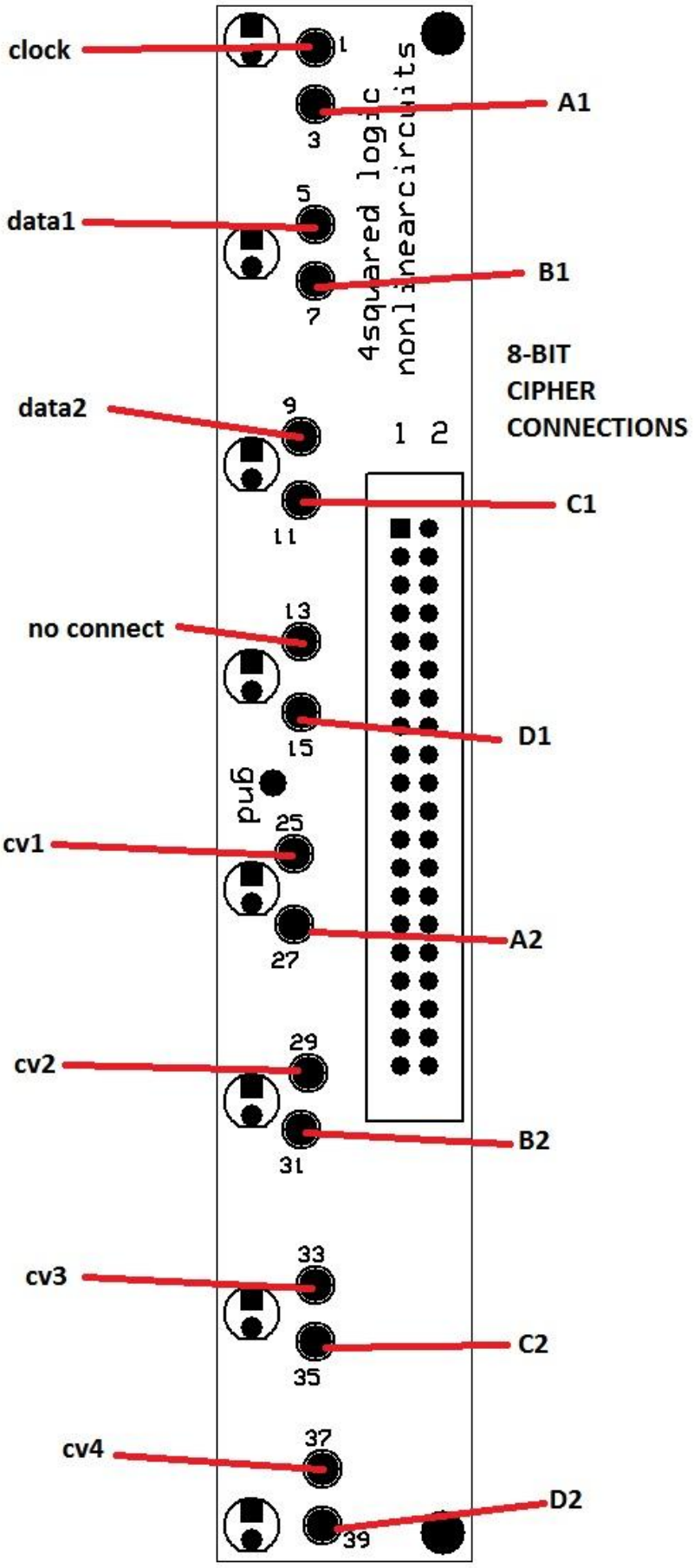
around 15 decoupling caps

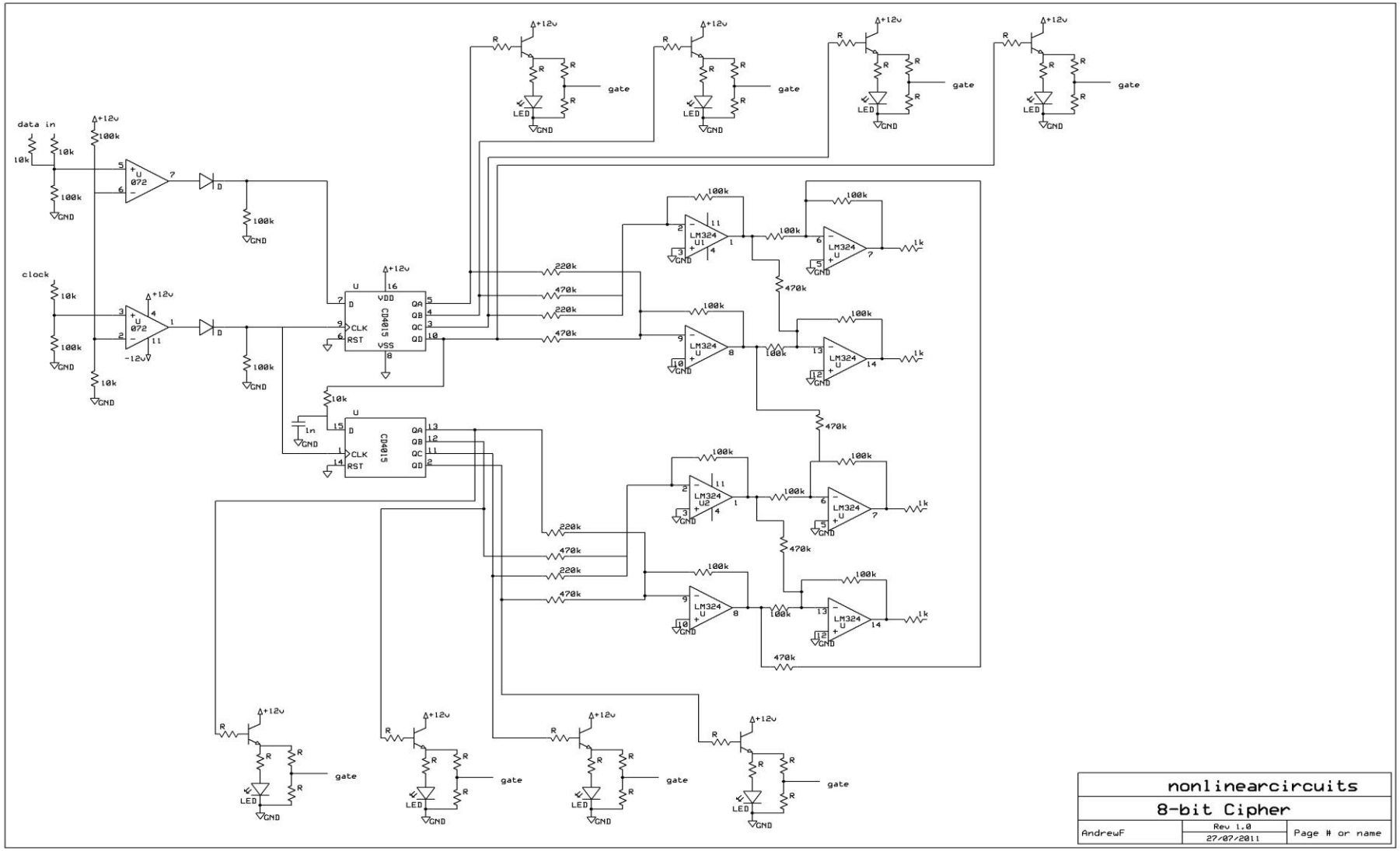
……and more.

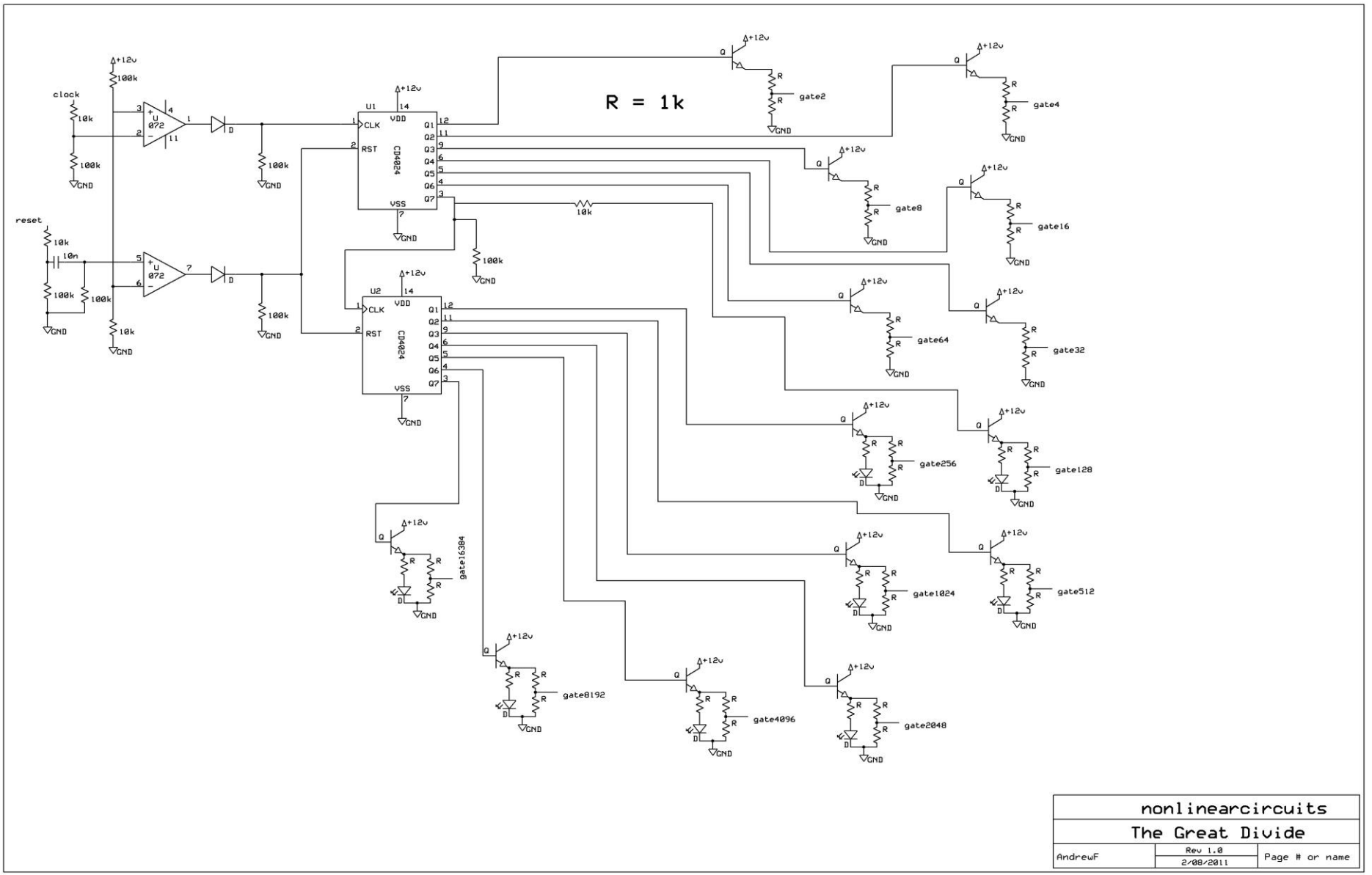

4024b
4024a
"Don't hate the media,
become the media" - Jello
nonlinearcircuits
4015 4024x2
10k
1N4004 x 2
unmarked res=100k
caps=10n-100n
+=1k all trannies=NPN



GREAT DIVIDE
CONNECTIONS


clock
1
A1
3
data1
5
B1
7
4squared logic
nonlinearcircuits
8-BIT
CIPHER
CONNECTIONS
data2
9
1 2
C1
11
no connect
13
D1
15
gnd
cv1
25
A2
27
cv2
29
B2
31
cv3
33
C2
35
cv4
37
D2
39


data in
clock
+12v
-12v
GND
gate
LED
R
100k
10k
220k
470k
1k
1n
U
072
CD4015
LM324
VDD
VSS
CLK
RST
QA
QB
QC
QD
D
nonlinearcircuits
8-bit Cipher
AndrewF
Rev 1.0
27/07/2011
Page # or name



nonlinearcircuits		
The Great Divide		
AndrewF	Rev 1.0 2/08/2011	Page # or name